REMARKS

Claims 1, 3 and 4 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **August 2, 2004**.

Objection to the Title

The Examiner has required a new, more descriptive title. The title has been amended to read: "ELECTRONIC PARTS PACKAGING STRUCTURE HAVING MUTUALLY CONNECTED ELECTRONIC PARTS THAT ARE BURIED IN AN INSULATING FILM".

Therefore, withdrawal of the objection to the title is respectfully requested.

Rejections under 35 USC §112, second paragraph

Claim 4 is rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, the Examiner is objecting to the phrase "a side surface of the via hole formed in the electronic parts except a bottom portion is covered with an inorganic insulating film". Claim 4 is described on page 9, lines 11-18, of the specification and shown in Figure 1D and 1K as an inorganic insulating film (14) formed in via hole (10b). However, in order to more clearly state that "a side surface of the via hole formed in the electronic parts is covered with an inorganic insulating

film except a bottom portion of the via hole is not covered with the inorganic insulating film", claim 4 has been amended. Therefore, withdrawal of the rejection of Claim 4 under 35 USC §112, second paragraph, is respectfully requested.

Claim Rejections under 35 USC §102(e)

Claims 1 and 2 are rejected under 35 USC §102(e) as being anticipated by Umetsu et al. (U.S. Patent Application Publication #2002/0127839A1).

The present invention is an electronic parts packaging structure in which a wiring substrate (40) having a base substrate (30) with a wiring pattern (32) contained therein a semiconductor chip (20) (electronic parts) is mounted on the wiring substrate (40). Bumps 11 on the semiconductor chip (20) are flip-chip bonded to a second wiring patterns (32a) of the wiring substrate (40). A second interlayer insulating film (34a) covers the semiconductor chip (20). Via holes (10b) are formed each having a depth that reaches the connection pad 10a on the element forming surface side of the semiconductor wafer (10). A third wiring patterns (32b) (overlying wiring patterns) are formed connected to the through electrodes (16) via the second via holes (34y).

Umetsu et al. describes a wiring board (5) and a circuit board (80) having a semiconductor chip (10). A semiconductor device (3) may be electrically connected to the circuit board (80) by mechanically connecting external terminals (90) to interconnecting pattern (82). Insulating material (22) is used to cover the semiconductor chip (10). Penetrating holes (24) are formed to penetrate

through at least a semiconductor chip (10). A metal layer (16) may be provided on the electrode (14).

Amended claim 1is characterized such that the electronic parts is flip-chip connected to a wiring substrate in the condition that the electronic parts is buried in an insulating film.

In amended claim 1, since thin electronic parts (150 μm or less) can be used, a total thickness of the electronic parts packaging structure can be reduced, and such packaging structure can respond to a higher density.

In Umetsu, through holes are formed in the semiconductor chip, but, the semiconductor chip is not buried in an insulating film, and the insulating film is not formed on the wiring substrate.

Additionally, in Umetsu, the metal layer (16) that the examiner points out to correspond to the overlying wiring pattern in claim 1 is formed on pad (14) (conductive layer), and is not formed on the insulating film that the semiconductor chip is buried.

Accordingly, the constitutions of Umetsu are different from the constitutions of amended claim 1. Also, technical idea that the semiconductor chip is packaged to be buried in the insulating film is nothing at all in Umetsu.

Therefore, claim 1 patentably distinguishes over the prior art relied upon by reciting,

> "An electronic parts packaging structure, comprising: a wiring substrate including a predetermined wiring pattern; an electronic parts, a connection terminal on an element forming surface of which is flip-chip connected to the wiring pattern; an insulating film in which the electric parts is buried, the insulating film formed on the electronic parts and the wiring substrate; a via hole formed in a predetermined

> portion of the electronic parts and the insulating film on the connection terminal; and an overlying wiring pattern formed on the insulating film and connected to the connection terminal via the via hole." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 1 and 2 under 35 USC §102(e) as being anticipated by Umetsu et al. (U.S. Patent Application Publication #2002/0127839A1) is respectfully requested.

Claim Rejections under 35 USC §103

Claims 3-7, insofar as claim 4 can be understood, are rejected under 35 USC §103(a) as being unpatentable over Umetsu et al. (U.S. Patent Application Publication #2002/0127839A1).

For the same reasons as discussed in regard to claim 1, amended claim 3 distinguishes over the prior art relied upon. In amended claim 3, since thin electronic parts (150 μm or less) can be used, a total thickness of the electronic parts packaging structure can be reduced, and such packaging structure can respond to a higher density.

In Umetsu, through holes are formed in the semiconductor chip, but, the semiconductor chip is not buried in an insulating film, and the insulating film is not formed on the wiring substrate.

Additionally, in Umetsu, the metal layer (16) that the examiner points out to correspond to the overlying wiring pattern in claim 3 is formed on pad (14) (conductive layer), and is not formed on the insulating film that the semiconductor chip is buried.

Therefore, claim 3 patentably distinguishes over the prior art relied upon by reciting,

> "An electronic parts packaging structure comprising: a wiring substrate including a predetermined wiring pattern; an electronic parts, a connection terminal on an element forming surface of which is flip-chip connected to the wiring pattern, and the electronic parts having a through electrode which is connected to the connection terminal via a first via hole formed in the electronic parts, on a back surface; an insulating film in which the electric parts is buried, the insulating film formed on the electronic parts and the wiring substrate; a second via hole formed in a predetermined portion of the insulating film on the through electrode; and an overlying wiring pattern formed on the insulating film and connected to the through electrode via the second via hole." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 3-7 under 35 USC §103(a) as being unpatentable over Umetsu et al. (U.S. Patent Application Publication #2002/0127839A1) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims1, 3 and 4, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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